

EEEN 3449

Test # 3 Spring 2007

Name: _____

1. Write a subroutine to create a delay of a multiple of 10 μs with a prescale factor equals to 16. Use Channel 1 for output compare. The minimum delay created by this subroutine is 10 μs . The delay to be created is equal to the value in **index register Y** multiplied by 10 μs , assuming that the E clock frequency is 24 MHz. Use the timer to control the delay, no PUSH & PULL from the stack. *Comment statement is a must for each of your statement.*

Solution:

;the following subroutine creates a delay of 10 μs

```
delay      movb    #$90,TSCR1
           movb    #$04,TSCR2
           movb    #$02,TIOS
           ldd     TCNT
           add     #15
           std     TC1
wait_lp2   brclr   TFLG1,$02,wait_lp2
           dbne   y,delay
           rts
```

Show your calculation for the # of counts:

$$\frac{24,000,000}{16} \times 10 \times 10^{-6} = 15$$

2. Supposing that we have the following instruction sequence to be executed by the HCS12, what will be the contents of the topmost four bytes of the stack after the execution of these instructions:

```
LDS      #$1500
LDAA    #$56
STAA    1, -SP
LDAB    #22
STAA    1, -SP
LDY     #0
STY     2, -SP
```

Answer : The topmost four bytes are \$00, \$00, \$16, and \$56.

\$00	Top first byte of the stack
\$00	Top second byte of the stack
\$16 = 22	Top third byte of the stack
\$56	Top fourth byte of the stack

3. Assume that the following setting was programmed before a new conversion is started:

- The conversion counter value in the ATD0STAT0 register is 4.
- The channel-select code of the ATD0CTL5 is 7.
- The conversion sequence limit of the ATD0CTL3 register is set to 6.
- The MULT bit of the ATD0CTL5 register is set to 1.

How would the conversion results be stored when the FIFO mode is selected or not selected?

Answer:

Analog Channel	Result stored in FIFO mode	Result stored in non-FIFO mode
AN7	ATD0DR4	ATD0DR0
AN0	ATD0DR5	ATD0DR1
AN1	ATD0DR6	ATD0DR2
AN2	ATD0DR7	ATD0DR3
AN3	ATD0DR0	ATD0DR4
AN4	ATD0DR1	ATD0DR5

4. Write an instruction sequence to configure the HCS9S12DP256 A/D converter with the following characteristics:
- $f_{osc} = 8 \text{ MHz}$
 - Channel AN0~AN3
 - A/D result right-justified
 - 8-bit resolution, unsigned result, continuous conversion
 - Four conversions in a sequence
 - Prescaler set to 2
 - Four cycles second state sample time, non-FIFO mode
 - Enable fast ATD flag clear, enable ATD interrupt
 - External falling edge triggered (at ATD7 pin)
 - Finish current conversion then freeze in background debug mode

Solution:

```

movb  #$E6 , ATD0CTL2      ; enable AD0, fast ATD flag clear, enable interrupt
movb  #$22 , ATD0CTL3      ; perform 4 conversions in a sequence, finish current
                                ; conversion then stop in freeze mode
movb  #$A0 , ATD0CTL4      ; 8-bit resolution, set prescaler to 2, 4 cycles second
                                ; stage sample time
ldy   #2                    ;20 micro second delay
jsr   delayby10us

```

Also need to write the value of \$A0 to the ATD0CTL5 register when starting to perform the ATD conversion.

5. Write a program to count the number of even number of an array of N 16-bit numbers. The array is stored at memory location from \$1010. N is no larger than 255. *Comment statement is a must for each instruction.*

Solution:

```

N          equ    20                ; array count
          org    $1000
even_cnt   rmb    1                ; the even count

          org    $1010                ; starting address of the array
arr        fdb    133,1200,1390,1900,1881,3939,2010,4080,9801,4592
          fdb    11,22,33,3333,3242,5435,8760,9800,2876,9601

          org    $1500
          ldy    #arr                ; use Y as the pointer to the array
          ldab   #N                  ; use B as the loop count
          clr    even_cnt
cnt_lp     brset  1,Y,$01,is_odd     ; check the LSB of the lower byte
          inc    even_cnt
is_odd     iny
          iny
          dbne   b,cnt_lp
          swi
          end

```

Registers related to the Output-compare Function

	7	6	5	4	3	2	1	0	
\$0040	IOS7	IOS6	IOS5	IOS4	IOS3	IOS2	IOS1	IOS0	TIOS
\$004D	TOI	0	0	0	TCRE	PR2	PR1	PR0	TSCR2
\$0044	Bit 15	14	13	12	11	10	9	Bit 8	TCNT(H)
\$0043	Bit 7	6	5	4	3	2	1	Bit 0	TCNT(L)
\$0046	TEN	TSWAI	TSFRZ	TFFCA	0	0	0	0	TSCR1
\$004E	C7F	C6F	C5F	C4F	C3F	C2F	C1F	C0F	TFLG1
\$0052	Bit 15	14	13	12	11	10	9	Bit 8	TC0(H)
\$0051	Bit 7	6	5	4	3	2	1	Bit 0	TC0(L)

TIOS: Timer Input-capture/Output-Compare Select Register
TSCR1: Timer System Control Register 1
TSCR2: Timer System Control Register 2
TFLG1: Timer Interrupt Flag 1 Register
TCNT: Timer Counter Register
TC0: TC register for Channel 0

Timer Counter Prescale Factor

PR[2:1:0]	Prescale Factor	PR[2:1:0]	Prescale Factor
000	1	100	16
001	2	101	32
010	4	110	64
011	8	111	128