

EEEN 3449

HW # 5

Due: April 15, 2009

There will be a quiz on this homework on 4/15/09.

1. Assuming that S8C~S1C (ATD0CTL3) are set to 0111 and CC~CA (ATD0CTL5) are set to 101, what is the conversion sequence for this setting?

Solution:

The first channel to be converted is AN5. Seven samples will be converted. The conversion sequence is as follows:

AN5, AN6, AN7, AN0, AN1, AN2, and AN3

2. Write an instruction sequence to configure the HCS12DP256 A/D converter with the following characteristics:
 - $f_{osc} = 8$ MHz
 - Channels AN0~AN3
 - A/D result right-justified
 - 8-bit resolution, unsigned result, continuous conversion
 - Four conversions in a sequence
 - Prescaler set to 2
 - Four cycles second stage sample time, non-FIFO mode
 - Enable fast ATD flag clear, enable ATD interrupt
 - External falling edge triggered (at ATD7 pin)
 - Finish current conversion then freeze in background debug mode.

Solution:

The instruction sequence to configure the AD0 to the desired setting is as follows:

```
movb #$E6 ,ATD0CTL2 ; enable AD0, fast ATD flag clear, enable interrupt
movb #$22 ,ATD0CTL3 ; perform 4conversions in a sequence, finish current
                        ; conversion then stop in freeze mode
movb #$A0 ,ATD0CTL4 ; 8-bit resolution, set prescaler to 2, 4 cycles second
                        ; stage sample time

ldy #2
jsr delayby10us
```

One also needs to write the value of \$A0 to the ATD0CTL5 register when starting to perform the ATD conversion.

3. Assuming that the following setting was programmed before a new conversion is started:

- The conversion counter value in the ATD0STAT0 register is 3.
- The channel-select code of the ATD0CTL5 is 5.
- The conversion sequence limit of the ATD0CTL3 register is set to 4.
- The MULT bit of the ATD0CTL5 register is set to 1.

How would the conversion results be stored when the FIFO mode is selected or not selected?

Solution:

Conversion results storage

analog channel	result stored in (FIFO mode)	result stored in (non FIFO mode)
AN5	ATD0DR3	ATD0DR0
AN6	ATD0DR4	ATD0DR1
AN7	ATD0DR5	ATD0DR2
AN0	ATD0DR6	ATD0DR3